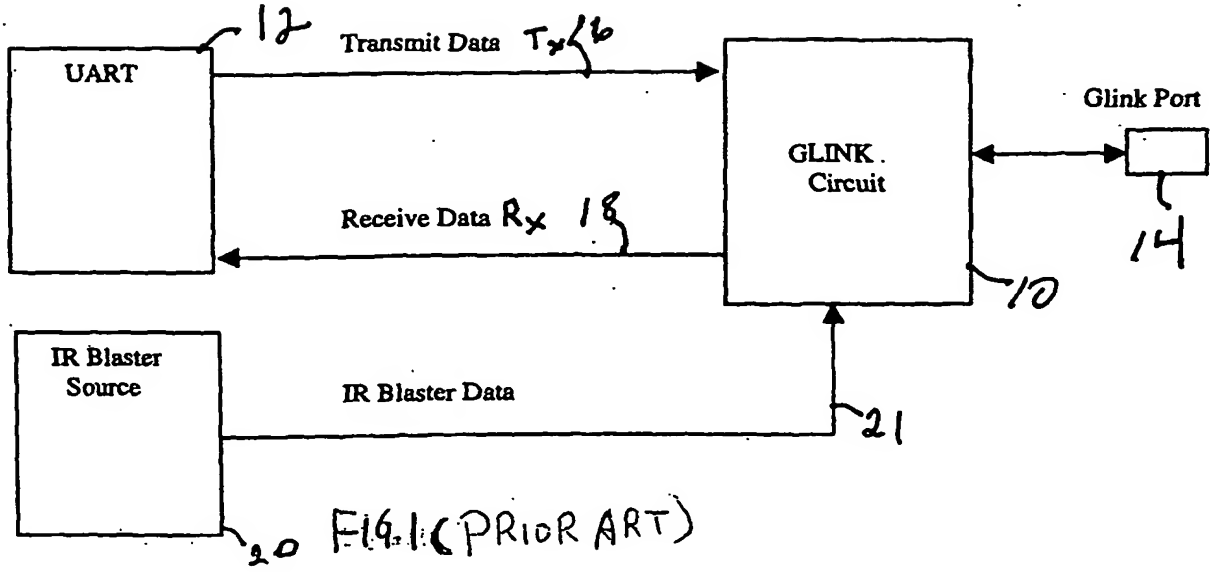

FIG. 1 (PRIOR ART)

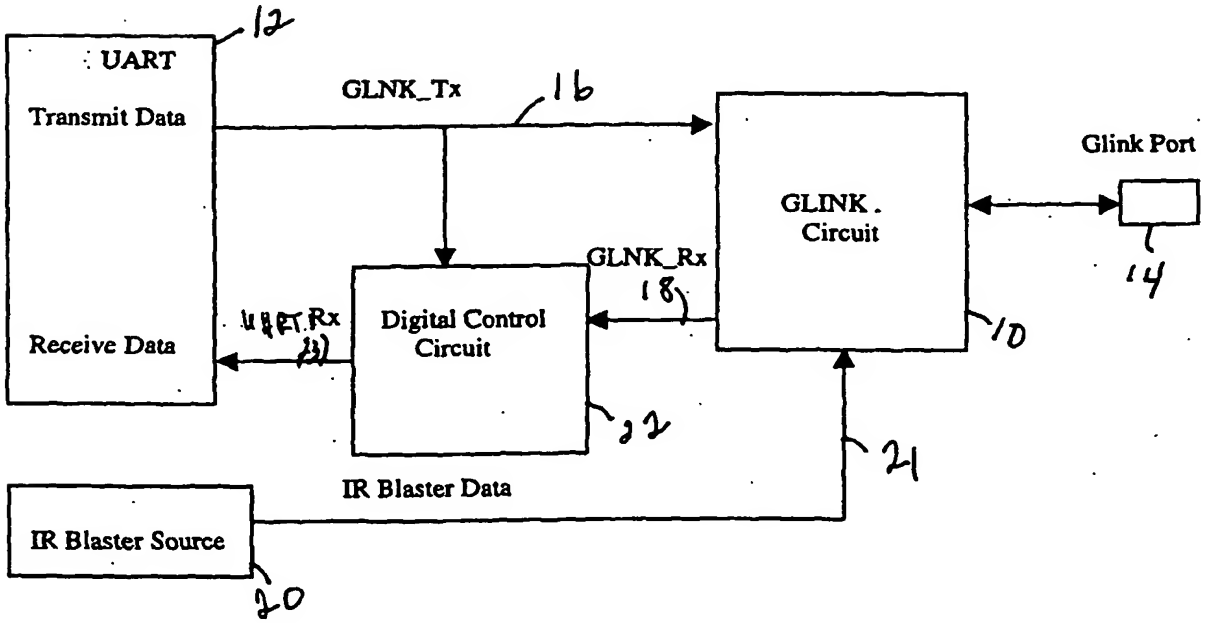

FIG. 2

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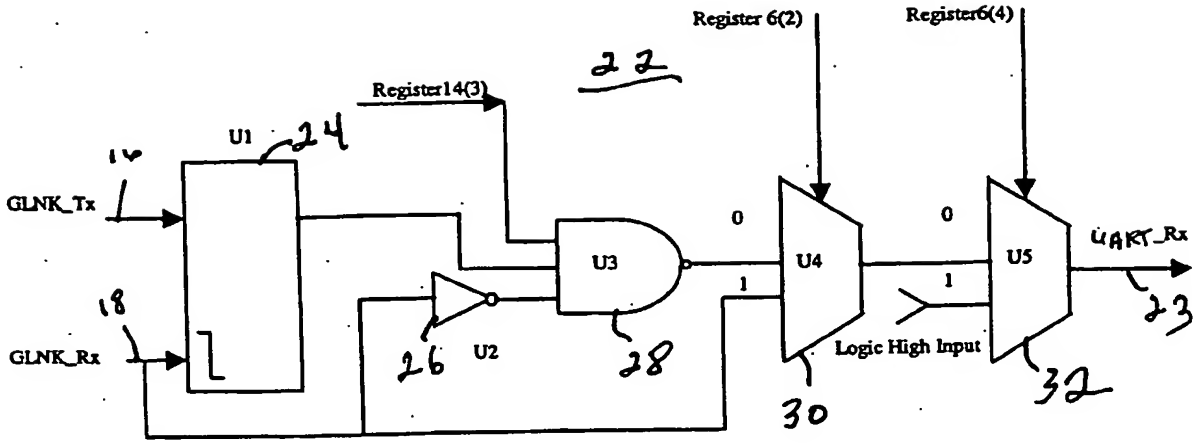

FIG. 3A

Digital Control Circuit							
Mode	CPLD Control Registers			CPLD Data Inputs		UART Input	Comments
Setup #	Register6(4)	Register6(2)	Register14(3)	GLNK_Tx	GLNK_Rx	UART_Rx	
1 (Mode 1)	0	0	1	1	X	=GLNK_Rx	Default Setting
2 (Mode 1)	0	0	1	0	X	LOGIC 1	Default Setting
3 (Mode 1)	0	0	0	X	X	LOGIC 1	IR Blaster Active
4 (Mode 2)	0	1	0	X	X	=GLNK_Rx	Configuration Test Mode
5 (Mode 3)	1	X	X	X	X	LOGIC 1	DETECTED DEMO PIN

X: don't care if level is logic high or low

FIG. 3B

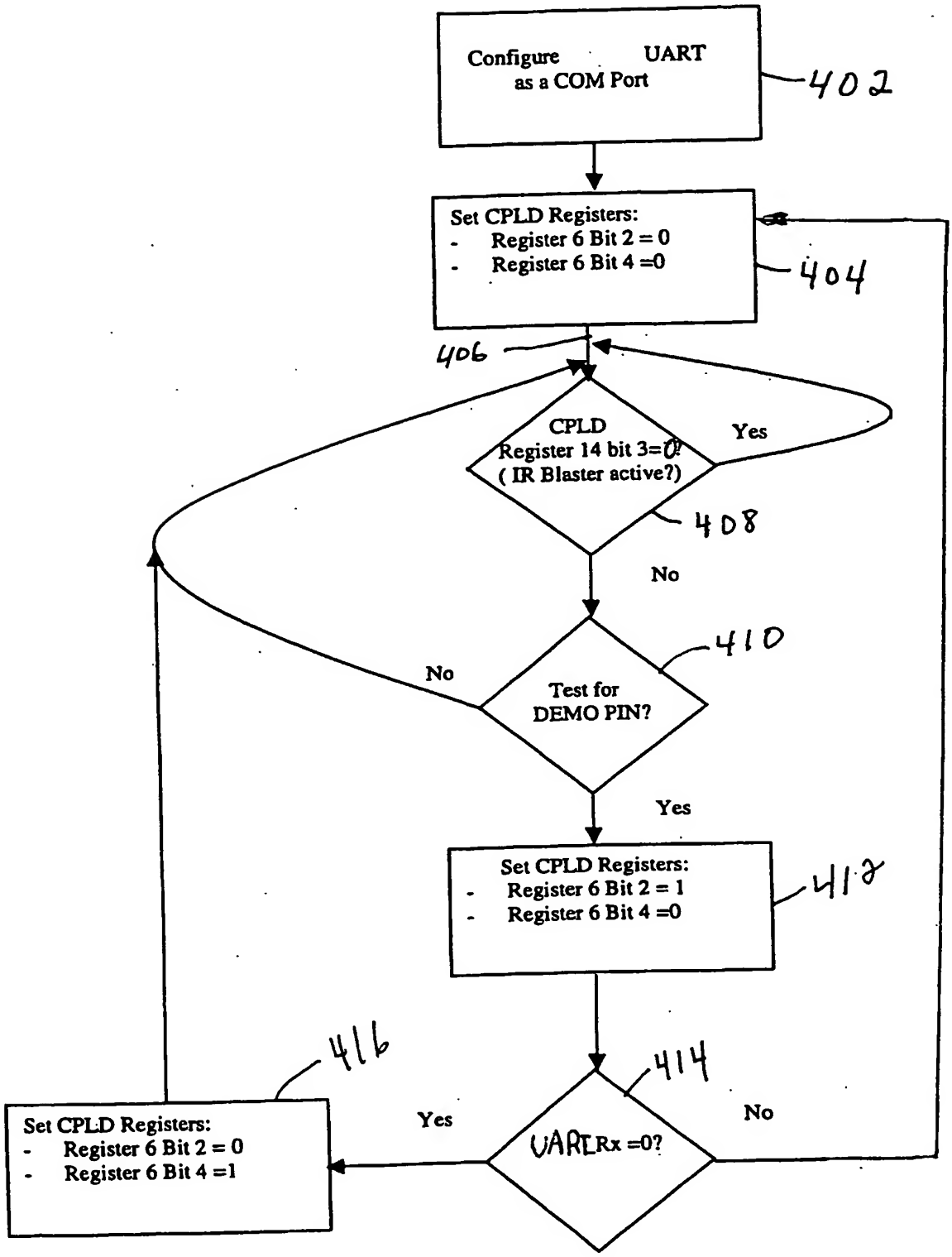
Configure UART as a COM Port
402
Set CPLD Registers:
- Register 6 Bit 2 = 0
- Register 6 Bit 4 =0
404
406
CPLD Register 14 bit 3=0? (IR Blaster active?)
Yes
408
No
Test for DEMO PIN?
410
No
Yes
Set CPLD Registers:
- Register 6 Bit 2 = 1
- Register 6 Bit 4 =0
412
414
UARTRx =0?
Yes
No
Set CPLD Registers:
- Register 6 Bit 2 = 0
- Register 6 Bit 4 =1
416

FIG. 4

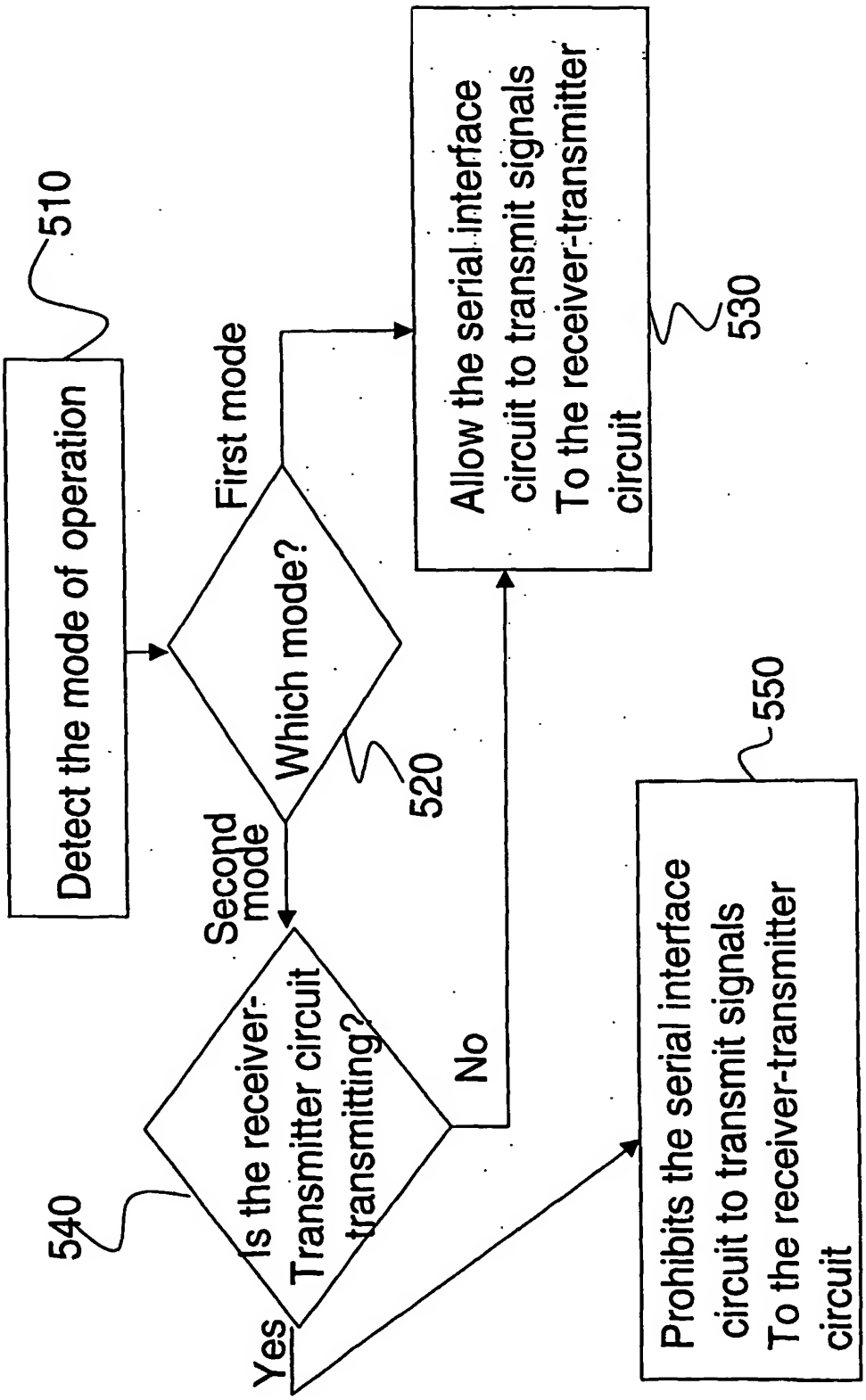
510
Detect the mode of operation
520
Which mode?
First mode
Second mode
530
Allow the serial interface circuit to transmit signals To the receiver-transmitter circuit
540
Is the receiver-Transmitter circuit transmitting?
No
Yes
550
Prohibits the serial interface circuit to transmit signals To the receiver-transmitter circuit

FIG. 5

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